

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A circuit for interfacing between a
2 first component operating at a first clock rate and a second
3 component operating at a second clock rate wherein said second
4 clock rate is higher than said first clock rate, said circuit
5 comprising:

6 a first buffer coupled to said first component, said first
7 buffer receiving and storing data received from said first
8 component at said first clock rate;

9 a second buffer coupled to said second component, said second
10 buffer supplying data recalled therefrom to said second component
11 at said second clock rate;

12 a copy/access controller connected to said first buffer, said
13 second buffer, and said second component and operable to copy data
14 from said first buffer to said second buffer when said first buffer
15 is substantially full, and further operable to prompt said second
16 component to access said second buffer when said data is copied
17 from said first buffer.

1 2. (Original) The circuit as set forth in Claim 1, wherein both
2 said first buffer and said second buffer are random-access
3 memories.

1 3. (Original) The circuit as set forth in Claim 1, wherein both
2 said first buffer and said second buffer are shift registers.

1 4. (Original) The circuit as set forth in Claim 1, wherein said
2 circuit is integrated onto a semiconductor die with one of said
3 first component or said second component.

5 to 14. (Canceled)